REMARKS

In the Office Action dated January 18, 2007, claims 1-18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,886,510 (Crespi) in view of U.S. Patent Application Publication No. 2004/0004483 (Hazelton).

Claim 1 describes a method for detecting an error condition associated with a load or a connection to the load comprising:

- during a first diagnosis phase determining whether the load or the connection to the load is in a normal operation condition or in an error condition, and
- if the load or the connection to the load is in an error condition, during a second diagnosis phase determining whether the error condition is an open load condition, short circuit condition to ground or a short circuit condition to a power supply,
- wherein the second diagnosis phase comprises changing a first parameter associated with the load in an attempt to escape from said error condition.

Preliminarily, it may be useful to give some further explanation on what is meant by "changing a first parameter associated with the load in an attempt to escape from said error condition". Reference will be made to the example in the specification but this is not to be construed as limiting on the claim but only as a means of explanation. In the example given in the description, the first parameter is given by the current, flowing in or out the sensor pin SP (see specification, page 9: 15-17). By changing this current, the voltage on the sensor pin can be changed (page 9: 22-23). In the no-error situation, the voltage at the pin is situated between the voltage levels VrefLO and VrefHI and in the error condition, the voltage at the pin is below VrefLO or above VrefHI (page 8: 30-32). When an error condition is detected during the first diagnosis phase of the method, a current is sent to the sensing pin SP, trying to change the voltage at the pin in a way that the voltage is again situated between the levels VrefLO and VrefHI (which normally is an indication of a non-error condition).

When the voltage at the pin is below VrefLO, a current is "sourced" from the pin SP, trying to increase the pin voltage and when the voltage at the pin is above VrefHI, a current is "sunk" into the pin SP, trying to decrease the pin voltage (page 10: 9-17). Depending on the error, this trial may be successful or not. This is only one example of what is expressed in claim 1 by the wording "in an attempt to escape from said error condition".

Crespi discloses a method for detecting an error condition associated with a load (LD) or a connection to the load. The method is a one step method, described in the passage of col. 4: 5-29. This passage of Crespi describes that four possible situations of the circuit (LD correctly connected or no-error condition, OUT short-circuited to ground, OUT short-circuited to supply and OUT open-circuit) correspond to four possible voltages at the node S (VS) : the first one below or equal to Vdd-Vth, the second one close to 0V, the third one equal to Vdd-Vth and the fourth one Vref, respectively. Vref is a voltage value, situated somewhere in the middle of the voltage range of the system, between the thresholds Vr1 and Vr2 of the used comparator systems (see Fig. 7 and 8 of Crespi).

In Crespi a current parameter is changed, in particular in the case of an OUT open-circuit. However, in Crespi the current brings the voltage at the node S not in the situation of no-error (which is around Vdd-Vth), but at a chosen reference voltage Vref. In Crespi, there is no "attempt" either, because, in the given situation, the voltage at the node S is always brought at the voltage Vref.

Claim 1 is thus distinct from Crespi because in Crespi there is no disclosure or suggestion of a second diagnosis phase and there is no disclosure of a parameter changing, as recited in claim 1.

Hazelton discloses a method for controlling and monitoring an electric load; the method can be subdivided in two steps: a first step in which an indication of a fault is obtained and a second step giving type and location of the fault (*see, e.g.,* ¶ [0011]). However, the parameter changing element of claim 1 is not disclosed or suggested in Hazelton.

To establish a *prima facie* case of obviousness (*see* M.P.E.P. § 2143 (8th ed., Rev. 5), at 2100-126):

- there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings; and

- the prior art references when combined must teach or suggest all the claim limitations.

In the present case, not one of the criteria above is met.

There is no motivation to combine Crespi and Hazelton. Each of the two references teaches a method for detecting errors or faults in a circuit on its own and it is not clear how such a combination should be done. Taking Crespi as the primary reference, where a method is disclosed to detect errors in a one step procedure, there is no motivation to take some teachings from Hazelton in order to come to a two-step process. If the motivation would be to add a degree of reliability, as seems to be suggested in the Office Action, a simple solution would be to repeat the Crespi process in order to see whether the results remain the same.

Thus, a combination of the teachings from Crespi and Hazelton with the teachings would not lead to the method proposed in claim 1. Normally, such a combination would lead to a three-step process and it is not clear whether both teachings could be combined in another way. Therefore, there existed no motivation or suggestion to combine Crespi and Hazelton.

As already explained above, the changing of a parameter element of claim 1 is not disclosed or suggested by the references. In the Office Action it is suggested that "such specific parameter changing(s) as found in one form or another, in the various dependent claims, would have been obvious as matters of attempting to recover from a load fault...". The attention is drawn to the fact that changing of a parameter cannot have as a consequence that the system is "recovered" from a load fault but that a possible consequence is that the voltage at the sensing pin is at a level corresponding with a no error condition of the load. Recovering from the load fault can thus not be a motivation for modifying the change of the current parameter according to Crespi into a change of the current parameter according to claim 1. Hazelton also fails to teach or suggest the element above. The hypothetical combination of Crespi and Hazelton thus fails to teach or suggest all elements of claim 1.

In view of the foregoing, a *prima facie* case of obviousness has not been established with respect to claim 1 over Crespi and Hazelton.

Independent claim 11 is similarly allowable over Crespi and Hazelton.

Dependent claims are allowable for at least the same reasons as corresponding independent claims.

Allowance of all claims is respectfully requested. The Commissioner is authorized to charge any additional fees and/or credit any overpayment to Deposit Account No. 20-1504 (BGC.0006US).

Respectfully submitted,

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